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Interfacing ISP1160x to Hitachi SH7709 RISC Processor

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Application Note

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1.0	Jan 2003	• First release.	Jason Ong

Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

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Note: ISP1160x denotes any Philips embedded USB host controller whose name starts with 'ISP1160'; this includes ISP1160A, ISP1160A1, and any future derivatives.

1. Overview

When ISP1160x is integrated into a personal digital assistant (PDA) or handheld personal computer (HPC), it is usually connected to the external bus interface of a Reduced Instruction Set Computer (RISC) processor. This application note will present some of the important issues in such a design, using as a concrete example the Hitachi SH7709 RISC processor.

2. ISP1160x Interface Signals to a RISC Processor Bus

The processor bus interface of ISP1160x is designed for a simple direct connection with a RISC processor. The data transfer can be done in the programmed I/O (PIO) or direct memory access (DMA) mode. The estimated maximum data transfer rate on the generic processor bus of ISP1160x is approximately 15 Mbyte/s. This is based on an ISP1160x internal clock frequency value of 48 MHz. To achieve the maximum data transfer rate on the host processor bus, ISP1160x contains a ping pong structured RAM that allows alternative access from the RISC processor or from the internal Host Controller. The Host Controller uses 2 kbytes of the ping memory and 2 kbytes of the pong memory in its allocated memory.

The main ISP1160x signals to consider for connecting to a Hitachi SH7709 RISC processor are:

- A 16-bit data bus (D[15:0]) for ISP1160x, which is "little endian" compatible.
- An address lines (A0) is necessary for the complete addressing of the ISP1160x internal registers:
  - **A0 = 0**—Selects the Data Port of the Host Controller
  - **A0 = 1**—Selects the Command Port of the Host Controller
- A $\overline{\text{CS}}$ line used for selection of ISP1160x in a certain address range of the host system. This input signal is active LOW.
- $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are common read and write signals. These signals are active LOW.
- A set of DMA channel standard control lines: DREQ, $\overline{\text{DACK}}$ and EOT. These signals have programmable active levels.
- An interrupt line INT, which is programmable as active on level or edge and HIGH or LOW.
- The CLKOUT signal has a maximum value of 48 MHz.
- The $\overline{\text{RESET}}$ signal is active LOW.

3. Hitachi SH7709

This section highlights the main features of the Hitachi SH7709 processor (a member of the SH-3 family) for connecting to ISP1160x.

This RISC processor contains two bus state controllers: one is used by the CPU and cache memory called Bus State Controller (BSC), and the other is used by the internal DMA controller called BSCP.

The BSC of the SH7709 will generate all control signals on the external processor interface that will be used for the ISP1160x connection. The BSC divides the physical address space into six areas; each has a maximum size of 64 Mbytes. Using one of the CS1–CS6 Chip Select signals provided on the external bus is a simple way to select a certain area allocated for a specific device.

Each area has several features that can be set by software:

- Bus size: 8, 16 or 32 bits can be independently set for each area.

- Number of wait cycles can be independently set for each area.
- Setting the type of space for each area will enable a direct connection to several possible types of memory: SRAM, DRAM, SDRAM, and burst ROM. The SH7709 will generate the necessary signals to control each of these types of memory.
- Each area can be used in either the little or big endian mode. For correct data alignment, matching data widths and matching endians are necessary. The ISP1160x connection requires a 16-bit or little endian configuration of the selected memory area.

Certain areas are normally reserved in a system design because of the presence of other system resources that are allocated in those specific areas. For example, the MS7709ASE Solution Engine board from Hitachi allows a simple connection of ISP1160x in area 2 or in area 5, by using the CS2 or CS5 signals. This is because other system devices do not use these two areas.

However, using as a selection one of the CSn signals without additional address selection logic may not be very efficient because this will not allow other devices to be included in the same memory area. A good example may be allocating ISP1160x to area 4, which is also used on the Hitachi MS7709ASE board by a Super I/O chipset and a 10BASE-T chipset, still leaving an available space of 32 Mbytes, which can be allocated to other devices. In this situation, adding a simple selection logic is necessary to include ISP1160x in a certain address space.

4. Considerations in Timing Diagrams and WAIT States

The following is a short study of the timing diagrams of the main bus cycles of both ISP1160x and SH7709.

The timing diagram of the external bus cycle of the SH7709 is based on the frequency of the system clock CKIO signal. In all operating modes of the CPG (clock pulse generator) of SH7709 (using an external oscillator, external clock input on EXTAL pins or CKIO pin as clock input), the CKIO bus clock frequency is always in the range of 10 to 40 MHz. Currently, in the majority of PDA designs, the most encountered frequency values of the CKIO signal are in the range of 20 to 25 MHz.

According to the ISP1160x datasheet specifications, a read cycle requires the following main timing parameters (the requirements of the write cycle are similar):

- t_{RL} = 32 ns ($\overline{RD}$ LOW pulse width—minimal value required by ISP1160x),
- t_{RHRL} = 140 ns ($\overline{RD}$ HIGH to next $\overline{RD}$ LOW—minimal value required by ISP1160x) and
- t_{RHDZ} = 5 ns ($\overline{RD}$ hold time, minimal value that can be expected from ISP1160x).
- t_{RC} = 172 ns (will result as a sum of t_{RL} and t_{RHRL})
- t_{SLDV} = 300 ns (will be determined by the sum of instructions executed by the host processor in between two successive bus cycles addressing ISP1160x).

For a detailed analysis of a timing diagram, consider the access of an ISP1160x internal register (for example, the Control Register of the Host Controller). Access of an ISP1160x internal register requires two phases: writing the address of the selected register into the Command Port; then only can data transfer access ($\overline{RD}$/$\overline{WR}$) take place.

The timing diagram in Figure 4-1 describes the two phases of accessing ISP1160x:

- The first phase is accessing the Command Port of ISP1160x, to write the address of the data port that will be accessed. In this phase $\overline{CS}$ is active, the data lines D[15:0] contain the desired address. The $\overline{WR}$ pulse will be activated and will latch the data. Note the value of t_{SLDV} that represents the minimum time required between occurrence of the first phase and the second phase.
- The second phase consists of the access (read or write) to the data port selected by the address latched in the previous phase. Two timing diagrams are combined again in this second phase: one for the read

access and one for the write access. A series of $\overline{RD}$ and $\overline{WR}$ pulses are shown in the diagram to define the timing requirements between two consecutive accesses to ISP1160x: t_{RHRL}, t_{WHWL}, t_{RC}, t_{WC} as specified in the datasheet.

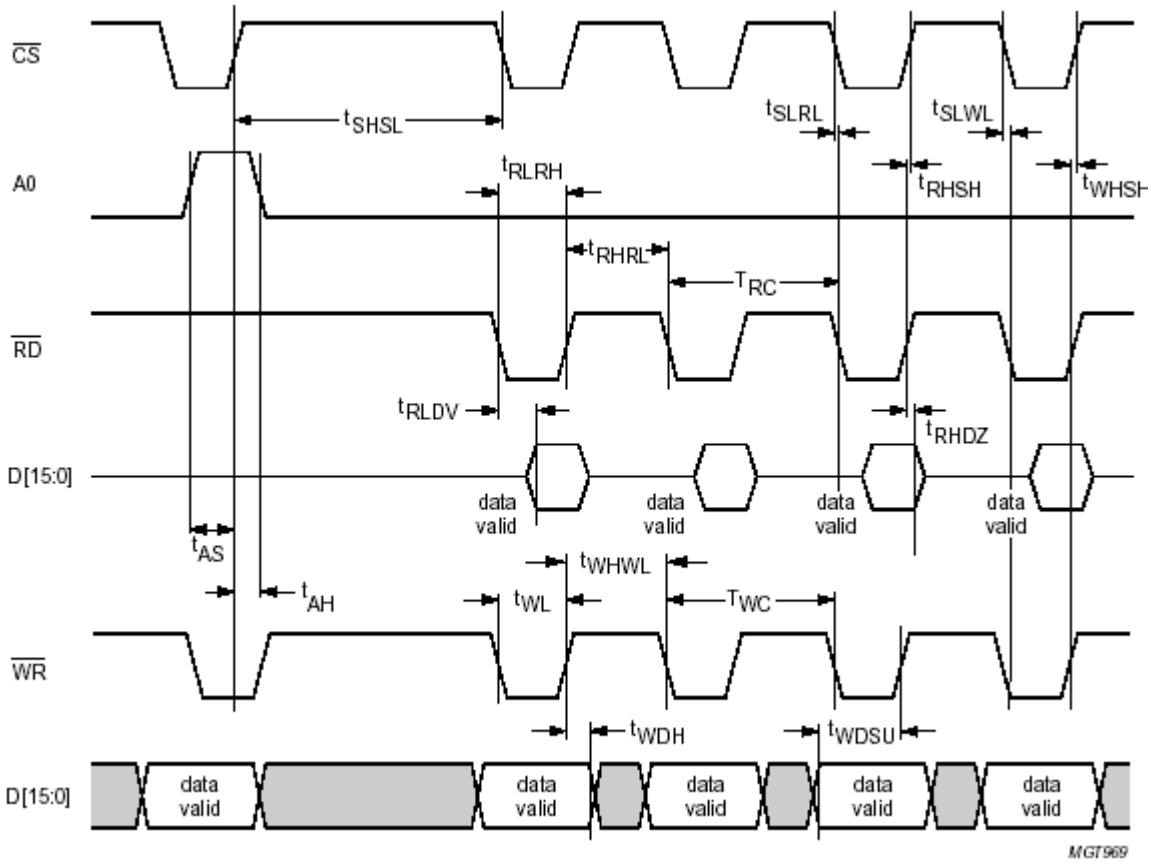


Figure 4-1: Programmed Interface Timing (16/32 bits Read/Write)

The approximate values of the ISP1160x parameters determined by the timing diagram of SH7709 in a standard bus cycle with no wait states and CKIO = 25 MHz (in the worst case scenario according to datasheet specifications) will be:

- t_{HRL} = 40 ns (SH7709 LOW pulse width),
- $t_{HRHRLmin}$ = 60 ns (estimated approximate minimal value of $\overline{RD}$ HIGH to next $\overline{RD}$ LOW), and
- t_{HRHDZ} = 0 ns ($\overline{RD}$ hold time, required by SH7709, in which data must still be valid after the rising edge of the $\overline{RD}$ signal).

When the ISP1160x connection area is defined as ordinary memory, ISP1160x will operate correctly even if CKIO = 33 MHz. Timing measurements show that inserting wait-states in the standard bus cycles of the SH7709 is unnecessary. Nevertheless, we will describe wait-state insertion, to cater for cases when faster bus cycles are used for accessing ISP1160x.

Inserting wait states into a $\overline{RD}$/$\overline{WR}$ bus cycle can be achieved by either hardware or software implementation. Both solutions will delay the rising edge of $\overline{RD}$/$\overline{WR}$ to the next CKIO cycle and will determine an elongation of the $\overline{RD}$/$\overline{WR}$ active LOW pulses that can be calculated as:

t_w = W x T(CKIO); where: (W) is the number of wait states desired

T(CKIO) is the cycle length of CKIO

Therefore, t_W is the additional pulse active time determined by the number of wait-states selected.

Note: the value of t_{RHRL} will not be modified by the number of wait states inserted by software programming a number of wait-states or even using the WAIT# input signal of the host processor. The value of t_{RHRL} must be calculated and correctly adjusted according to the number and length of instructions executed by the SH7709 between two successive accesses to the ISP1160x registers.

The solution described earlier for wait-state insertion in a bus cycle is simple and preferred in this configuration, if additional wait states are necessary. SH7709 allows insertion of a certain number of wait-states in a normal bus cycle by programming certain values into its internal *WCR2 register*. In this case, using the external WAIT signal of SH7709 is not necessary, as a predefined number of wait states will be inserted in each bus cycle, ensuring the minimum $\overline{RD}$ and $\overline{WR}$ pulse lengths as specified in the ISP1160x datasheet. This method allows the designer to use a minimal hardware implementation of the whole system. The number of wait states can be differently defined for each of the six areas contained in the physical address space of SH7709. Programming the wait state control register *WCR2* to insert a number of wait states for a slower device allocated in a certain area will not influence other faster resources selected in a different area.

5. Using Interrupts

ISP1160x generates an interrupt on INT. Occurrence of this interrupt depends on the setting of the interrupt register.

The INT signal can be directly connected to an available SH7709 IRQ signal. Choosing IRQ0—IRQ4 pins of SH7709 as interrupt input lines connected to INT of ISP1160x will allow SH7709 to wake up from standby status when any of these lines becomes active. In this case, you must use a 32 kHz crystal connected to the XTAL2 or EXTAL2 pin and a battery connected to the RTCVCC pin of SH7709.

The INT of ISP1160x can be programmed as active on level or edge and HIGH or LOW, as specified in the *HcHardwareConfiguration* Register.

The Hitachi SH7709 also allows sensing each interrupt on the rising or falling edge or on the LOW level, by programming with the desired values the bits of the *Interrupt Control Register*; individual control of the characteristics of each interrupt line is possible. It is necessary to match the settings of the ISP1160x interrupt line INT with the settings of the SH7709 IRQ line.

An interrupt on an SH7709 IRQ line is detected on the falling edge of the CKIO clock.

6. DMA Operation

ISP1160x'.s DMA handler —which is used by by the Host Controller—can work in the DACK mode or in the 8237 mode by using an EOT signal (End of Transfer), according to the bits setting of the *Hardware Control* registers. The DACK mode will be used when connecting ISP1160x to the Hitachi SH7709 RISC processor. To defime the parameters of the DMA operation (transfer counter enable, DMA enable, burst length) of the Host Controller, the *HcDMAConfiguration* and *HcTransferCounter* registers must be programmed. Details regarding programming DMA registers can be found in the ISP1160x datasheet and in the *ISP1160x Embedded Programming Guide*.

SH7709's DMA controller (DMAC) includes four DMA channels. Note: external requests (from the DREQn pins) are accepted from only channels 0 and 1. An interrupt request can be generated to the CPU after transfer ends by a specified count.

The flexible interfaces of ISP1160x and SH7709 allow signal connection of the ISP1160x DMA channels to the SH7709. This is done by connecting the DREQ and $\overline{DACK}$ signals of ISP1160x to the DREQ0 and DACK0 signals of SH7709, respectively. SH7709's DMAC allows DREQ to be detected on the falling edge or LOW level to be selected. The DACK output can be programmed as active LOW or HIGH, and the DACK-*only* mode is supported. These settings are contained in the respective *DMA Channel Control* register of SH7709. The control signals of the

ISP1160x DMA channels have programmable active levels, determined by the settings of the *HcHardwareConfiguration* Register of the Host Controller.

The EOT signal of ISP1160x is not used in this configuration because this mode is not implemented in the DMAC of SH7709 and there is no corresponding pin on the DMAC interface. A pull-up resistor must be provided on the EOT pin, if it is still not connected.

As shown in the following timing diagram, by asserting the $\overline{DACK}$ signal, the host system will allow data transfer to take place, allocating the bus for ISP1160x. Both $\overline{RD}$ and $\overline{WR}$ data transfer cycles are contained in the timing diagram. The $\overline{CS}$ signal is not used by ISP1160x'.s internal selection logic. The $\overline{DACK}$ signal will be used to define the bus owner that issued DREQ and is currently involved in the data transfer. No other system resource will be accessed as long as the DMA cycle is in progress and occupies the bus. The $\overline{DACK}$ active LOW pulses determine the time allocated to the DMA data transfer.

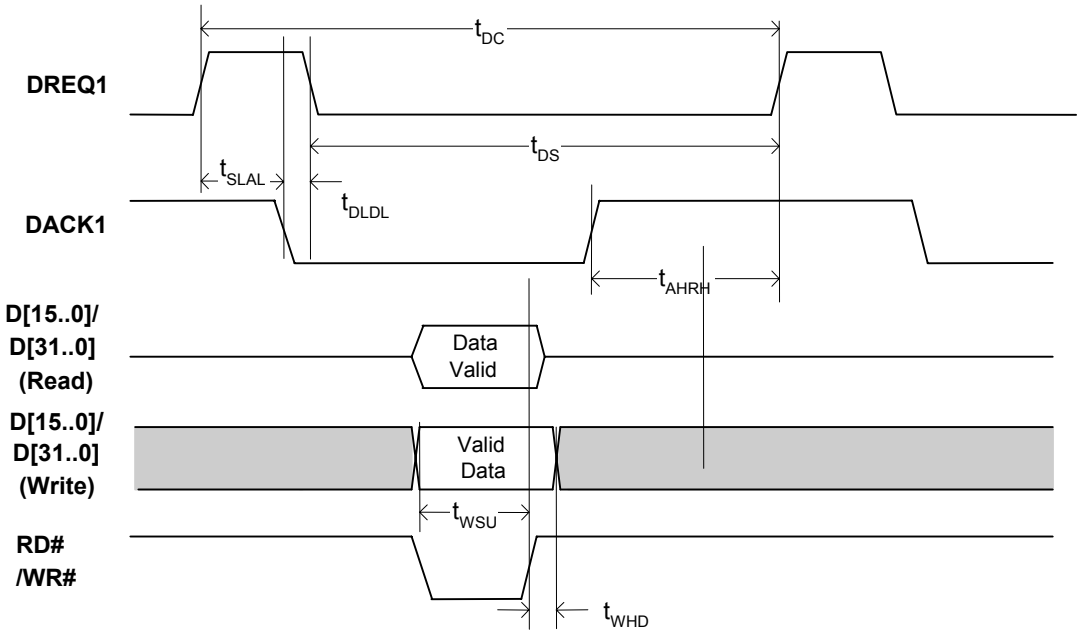


Figure 6-1: Host Controller Single Cycle Burst DMA Timing

The timing diagram of SH7709 specifies t_{DRQS} = 12 ns (DREQ setup time) and t_{DRQH} = 8 ns (DREQ hold time) relative to a falling edge of CKIO. If the DRQ signal generated by ISP1160x does not meet the t_{DRQS} timing in the current bus cycle, it will be sensed on the next falling edge of CKIO and the DACK will be generated accordingly.

The requirement t_{DRQH} = 8 ns is determined by the sum of DACK delay time from the falling edge of CKIO and the time between DACK is driven LOW by SH7709 until DREQ is deactivated by ISP1160x (t_{DLDL}). Since t_{DLDL} is in the range of10 to 21 ns, the requirement t_{DRQH} = 8 ns will be always satisfied.

A DMA burst access of up to 8 cycles for ISP1160x host DMA handler can be defined in the *HcDMAConfiguration* Register.

If necessary, add wait states to the basic DMA cycle to create longer $\overline{RD}$/$\overline{WR}$ and DACK pulses. Wait states can be inserted in the same way as described in Section 4.

7. Suspend and Resume

You can enable ISP1160x to enter the Reset, Resume, Operational and Suspend functional states by programming the *HcControl* Register.

Another way to wake up ISP1160x from the suspend mode is to use the input signal H_WAKEUP. This signal may be connected to any available I/O port line of the SH7709.

Monitoring the H_SUSPEND pin can determine the actual status of ISP1160x, without having to access the internal status registers. Connecting this signal to any available I/O port of the SH7709 is an easy way to determine the status of ISP1160x.

8. Schematic Diagram

The following schematic diagram shows the connection of ISP1160x to a SH7709 processor in a minimal hardware configuration.

In the example schematic, ISP1160x is simply selected by CS5 (in a more complex configuration some glue logic may be required to generate a CS signal composed of CSn and several address lines of the host system).

To correctly access ISP1160x, it is assumed that area 5 is programmed for the SRAM memory type and 16-bit accesses.

The DREQ and $\overline{\text{DACK}}$ lines are directly connected to the DREQ and DACK lines of the SH7709 DMA channel 0. The EOT signal, which is not used in this configuration, is connected to a pull-up resistor to keep this input pin in a controlled inactive logic state.

The WAKEUP and SUSPEND pins are connected to the I/O port PTC of SH7709. A direct control is possible using this configuration: the SUSPEND state of ISP1160x can be directly monitored and an immediate WAKEUP can be obtained without accessing the ISP1160x internal registers. An alternative method to determine ISP1160x WAKEUP is using $\overline{\text{CS}}$ signal, as shown in Section 7.

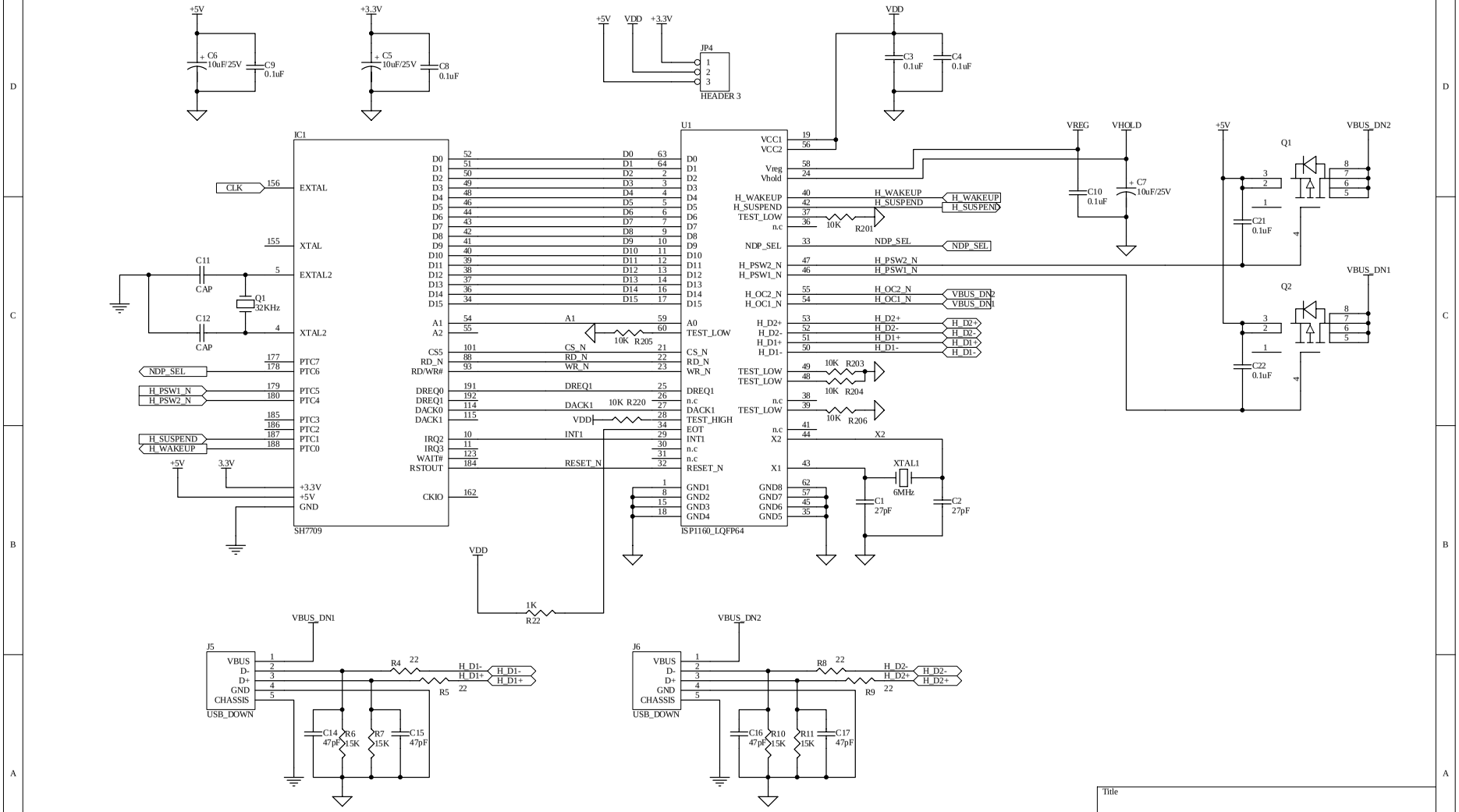
Pins $\overline{\text{H\_PSW1}}$ and $\overline{\text{H\_PSW2}}$ are connected to lines 4 and 5 of the same I/O port. This connection creates an alternative way to determine the power status of each of the downstream ports.

The SH7709 port C pins are multiplexed pins, having multiple functions. To use these pins as desired (input/output ports) correct programming of the *Port C Control* Register of SH7709 is required for setting the port function and the correct direction (input or output).

ISP1160x uses the input signals $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ to detect an overcurrent on the downstream ports. Because separate overcurrent detection and protection circuits are implemented for each downstream port in ISP1160x, so when an overcurrent on a downstream port is detected, power will be turned off at that port only. Connecting the voltages of the two downstream ports VBUS_DN1 and VBUS_DN2 to the $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ pins enables detection of the current value by sensing the voltage drop on Q1 and Q2 that are MOS transistors with very low switch-on resistance Rds(on). Q1 or Q2 is selected, depending on the desired maximum current value, and this determines the value of Rds(on). For example, if the allowed maximum current is approximately 0.5 A, a voltage drop of 75 mV will trigger the overcurrent circuitry and Rds(on) of approximately 150 MΩ will result. Connecting the ISP1160x input pins $\overline{\text{H\_OC1}}$ and $\overline{\text{H\_OC2}}$ to +5 V will disable the internal overcurrent protection of ISP1160x. You can opt for an external overcurrent protection circuit.

Selection of the number of downstream ports can be done in this configuration by programming the output PTC6 of the SH7709 to a certain value. This will determine the desired value on the NDP_SEL input signal of ISP1160x, and one or two downstream ports will be selected accordingly.

The $\overline{\text{RESET}}$ input signal of ISP1160x is given by the RSTOUT signal generated by SH7709.



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9. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1160 Embedded Universal Serial Bus Host Controller* datasheet
- *ISP1160A1 Embedded Universal Serial Bus Host Controller* datasheet
- *ISP1160x Embedded Programming Guide.*

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